REMARKS

REQUEST FOR RECONSIDERATION OF RESTRICTION REQUIREMENT TO ESTABLISH RIGHT OF PETITION

Applicant hereby requests reconsideration of the final requirement of restriction.

Rejections Under 35 U.S.C. §112, Second Paragraph.

Claims 8, 14 and 18 have been amended to address this ground of rejection.

Rejection of Claims 8, 9, 12 and 13 Under 35 U.S.C. §103(a), based on U.S. Patent No. 4,679,304 (*Bois*) in view of Japanese Patent Publication 62-216268 (A) (*Goto*) and further in view of U.S. Patent No. 5,731,221 (*Kwon*)

The invention of claim 8 is directed to a manufacturing method of a semiconductor device. The method includes etching the stacked film and the first oxide film to form a plurality of stacked film patterns and oxidizing the semiconductor substrate to form a second oxide film on a surface of the semiconductor substrate sandwiched between adjacent said stacked film patterns. The second oxide film has a film thickness thicker than the first oxide film. The method further includes forming a side wall mask film on a side of the stacked film patterns and removing the portion of the second oxide film sandwiched between the mask patterns to form a trench. The trench is filled with an insulating film.

As is well known, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

Because the rejection has not shown the necessary suggestion of motivation to combine the reference teachings, a prima facie case of obviousness has not been established.

It is well established that the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. This burden can be satisfied only by showing some objective teaching in the prior art or that knowledge general available to one or ordinary skill in the art that would lead the individual to combine the relevant teachings of the references.[1]

[1] In re Fritch, 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992).

Further, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.[2]

The rationale for modifying *Bois* in view of *Goto* is set forth below.

> It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Japan '268 to enable formation of the LOCOS mask of Bois.[3]

This rationale does show sufficient motivation as it only states the proposed modification relied upon, and presents no objective teaching in the prior art or generally available knowledge that suggests the desirability of the combination. In fact, the references are believed to teach away from the proposed combination.

Bois is directed to isolation zones formed by a removable nitride mask. That is, in *Bois*, once isolation zones have been formed, the mask is removed.[4] In contrast, *Goto* is directed to forming field oxide between gate electrodes.[5] As is well known, conventional gate electrodes are retained on a semiconductor device in order to form transistor gates. Thus, modifying *Bois* to incorporate the gate structures of *Goto* would change the principle operation of *Bois*. *Bois* would now include gate electrode structures, rather than removable isolation masks. As is well established, if a proposed modification or combination would change the principle operation of the prior art invention being modified, the teachings of the references are not sufficient to render the claims prima facie obvious.[6]

For these reasons, there is no motivation for combining *Bois* and *Goto*, as proposed in the rejection.

Similarly, motivation is also lacking for adding *Kwon* to the combination of *Bois* and *Goto*.

The rationale for modifying *Bois* and *Goto* further with *Kwon* is set forth below.

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[2] In re Mills, 16 USPQ2d 1430 (Fed. Cir. 1990)
[3] See the Office Action, dated 11/1/02, Page 3.
[4] See *Bois*, FIG. 5, Col. 4, Lines 4-7.
[5] See *Goto*, English Abstract, which indicates a conductive film is patterned to form a gate electrode that may be flattened.

> It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Kwon to enable formation of trench 10 of Bois.[7]

Again, the above rationale only states the proposed modification relied upon, and presents no objective teaching in the prior art or generally available knowledge that suggests the desirability of the combination. Thus, a prima facie case of obviousness cannot have been established for claim 8.

Claim 12, which depends from claim 8, recites that a second oxide film is approximately 20 to 50 nm thicker than the first oxide film. The rejection of claim 12, relies on the following rationale.

> Choice of particular LOCOS thickness of the LOCOS film would have been within the scope of one of ordinary skill in the art as a matter of routine optimization.[8]

Applicant rebuts the above rationale by pointing to the results achieved by such a thickness, as clearly set forth in Applicant's specification. Applicant's specification indicates that such a thickness range may result in (1) an advantageous ratio between a control capacitance and a substrate capacitance and (2) increase in distance between a floating gate edge and a shallow trench isolation (STI).[9] Such results are completely unexpected with reference to the limited teachings of the prior art.

Claim 13 recites that a stacked film can include a stopper film that provides a stopper for a chemical mechanical polishing step.

No grounds of rejection were provided for this claim.[10] Accordingly, a prima facie case of obviousness cannot have been established for this claim.

For all of these reasons, the rejection of claims 8, 9, 12 and 13, is traversed.

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[6] In re Ratti, 123 USPQ 349 (CCPA 1959).
[7] See the Office Action, dated 11/1/02, Page 3.
[8] See the Office Action, dated 11/1/02, Page 3.
[9] See the Specification, Page 10, Lines 5 to 8 and Page 12, Lines 7 to 16.

Rejection of Claim 10 Under 35 U.S.C. §103(a), based on *Bois* in view of *Goto*, further in view *Kwon*, and further in view of U.S. Patent No. 5,106,772(*Lai*)

To the extent that this ground of rejection relies on *Bois* in view of *Goto*, further in view *Kwon*, Applicant incorporates by reference herein the comments set forth above for claim 8.

In addition, Applicant adds that the motivation necessary for such a combination is lacking in the rejection.

The rationale for modifying *Bois*, *Goto* and *Kwon* further with *Lai*, is set forth below.

> It would have been within the scope of one of ordinary skill in the art to combine the teachings of the combination and those of *Lai* to enable EEPROM formation.[11]

As in the previous rejections, this rationale does not present some teaching of the prior art or generally available knowledge. Applicant believes the prior art clearly teaches away from combining *Bois* with *Lai*, for the same essentially reasons that a combination of *Goto* with *Bois* cannot be obvious. Namely, that *Bois* teaches isolation masks that are removed, and *Lai* teaches EEPROM gates, which are retained.

Rejection of Claim 11 Under 35 U.S.C. §103(a), based on *Bois* in view of *Goto*, further in view *Kwon*.

Claim 11 recites that a side wall mask film includes a nitride film.

In rejecting claim 11, the Examiner has taken official notice that nitride spacers as part of a hard mask were known prior to Applicant's invention. Applicant seasonably traverses this statement and requests the citation of references in support of the claim. Such references should show that the use of nitride spacers *as recited in Applicant's* claim is considered obvious.

Applicant notes the references relied upon to show Applicant's side wall spacer, *Kwon*, explicitly teaches spacers of polysilicon, and not nitride[12] – and hence explicitly teaches away from Applicant's claim limitations. Thus, any well known teaching relied upon would have to

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[10] The Office Action, dated 11/1/02, lists claim 13 in the rejection, but provides no grounds for rejection. Specifically, the limitations of claim 13 are never discussed.

[11] See the Office Action, dated 11/1/02, Page 4.

[12] See *Kwon*, FIG. 1B, and Col. 1, Lines 56-59.

objectively suggest the substitution of nitride spacers for polysilicon spacers in such an arrangement.

Rejection of Claims 14 and 15 Under 35 U.S.C. §102(b) based on *Bois*.

The Office Action has presented no reasons or rationale for this ground of rejection.[13] Thus, anticipation cannot have been established for these claims and this ground of rejection is traversed.

Rejection of Claims 16-20 Under 35 U.S.C. §103(a), based on *Bois* in view of *Lai*.

A prima facie case of obviousness cannot exist for these claims. The rejection of claims 16-20 applies the grounds of rejection for claims 14 and 15. However, as noted above, no grounds were presented for claims 14 and 15. Thus, this ground of rejection is also traversed.

[13] See the Office Action, dated 11/1/02, Page 4.

Claims 8, 14, 15, and 18 have been amended, not in response to the cited reference, but to more clearly claim the invention. The present claims 8-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Version With Markings to Show Changes Made

In the Claims.

8. (Amended) A manufacturing method of a semiconductor device, comprising the steps of:

forming a first oxide film on a surface of a semiconductor substrate;

depositing a stacked film including a first conductive layer in contact with the first oxide film;

etching the stacked film and the first oxide film to form a plurality of stacked film patterns arranged on the semiconductor substrate;

oxidizing the semiconductor substrate to form a second oxide film on a surface of the semiconductor substrate sandwiched between adjacent **said** stacked film patterns and a surface of the semiconductor substrate below end portions of the stacked film patterns wherein the second oxide film has a film thickness thicker than the first oxide film;

forming a side wall mask film on a side of the stacked film patterns to form mask patterns including the stacked film patterns;

removing the portion of the second oxide film sandwiched between the mask patterns and a portion of the underlying semiconductor substrate using the mask patterns as a mask to form a trench in the semiconductor substrate; and

filling the trench with an insulating film.

14. (Amended) A manufacturing method of a semiconductor device, comprising the steps of:

forming a first oxide film on a surface of a semiconductor substrate;

depositing a stacked film including a first **[stopper]** layer on the first oxide film;

etching the stacked film and the first oxide film to form a plurality of stacked film patterns arranged on the semiconductor substrate;

oxidizing the semiconductor substrate to form a second oxide film on a surface of the semiconductor substrate sandwiched between adjacent stacked film patterns and a surface of the semiconductor substrate below end portions of the

stacked film patterns wherein the second oxide film has a film thickness thicker than the first oxide film;

removing the portion of the second oxide film sandwiched between the **[mask]** **stacked film** patterns and a portion of the underlying semiconductor substrate using the stacked film patterns as a mask to form a trench in the semiconductor substrate; and

filling the trench with an insulating film.

15. (Amended) The manufacturing method of a semiconductor device according to claim 14, wherein:

the step of filling the trench with an insulating film includes forming the insulating film to have a top surface having a height that essentially matches with a height of the first **[stopper]** layer.

18. (Amended) The manufacturing method of a semiconductor device according to claim 16, wherein:

the insulating film has a top surface **[that]** substantially **[matches]** **even** with a top surface of the first electrode.